

Amendments to the Claims

1. (CURRENTLY AMENDED) A reading circuit for reading a memory cell having a single bit line and a corresponding reference cell, comprising:

- a first and second cascode circuit (~~24; 25~~) each having an input terminal (~~24a; 25a~~) and two output terminals (~~24b, 24e; 25b, 25e~~) respectively said input terminals (~~24, 25~~) being adapted to be connected to a bit line of said memory cell and a corresponding reference bit line of said reference cell, respectively,

- a first and second current mirror circuit (~~26, 27~~) having a first and second terminal (~~26a, 26b; 27a, 27b~~), respectively,

wherein said first terminal (~~26a~~) of said first current mirror circuit (~~26~~) is coupled to said first output terminal (~~24b~~) of said first cascode circuit (~~24~~) and said second terminal (~~26b~~) of said first current mirror circuit (~~26~~) is coupled to said second output terminal (~~25e~~) of said second cascode circuit (~~25~~),

wherein said first terminal (~~27a~~) of said second current mirror circuit (~~27~~) is coupled to said first output terminal (~~25b~~) of said second cascode circuit (~~25~~) and said second terminal (~~27b~~) of said second current mirror circuit (~~27~~) is coupled to said second output terminal (~~24e~~) of said first cascode circuit (~~24~~); and

a tri-state buffer (~~28~~) coupled between the second terminals (~~26b, 27b~~) of said first and second current mirror circuits (~~26, 27~~), wherein said tri-state buffer (~~28~~) having bit invert capabilities.

2. (CURRENTLY AMENDED) Reading circuit according to claim 1, wherein

said first and second cascode circuits (~~24, 25~~) are adapted as folded cascodes each having two transistors coupled at their respective sources, wherein said input terminals (~~24a, 25a~~) of said first and second cascode circuits (~~24, 25~~) are coupled to said sources of said transistors of said cascode circuits (~~24, 25~~), respectively.

3. (CURRENTLY AMENDED) Reading circuit according to claim 1, wherein

- a ratio of the outputs from said first and second output terminals ~~(24b, 24c, 25b, 25c)~~ of said cascode circuits ~~(24, 25)~~ is adapted as 1:m, m being larger than or equal to 1, and
- said first and second current mirror circuits ~~(26, 27)~~ are configured having a n:1 current transfer ratio, n being larger than or equal to 1.

4. (CURRENTLY AMENDED) Reading circuit according to claim 3,
wherein

the current transfer factor n of said current mirror circuits ~~(26, 27)~~ is larger than the output ratio factor m of said cascode circuits ~~(24, 25)~~.

5. (CURRENTLY AMENDED) Reading circuit according to claim 1,
wherein

said tri-state buffer ~~(28)~~ is configured as a SRAM cell.

6. (CURRENTLY AMENDED) An integrated circuit including a memory
having memory cells and reference cells, comprising:

- memory bit lines ~~(BL)~~,
- at least one reference bit line ~~(BL_R)~~,
- at least one reading circuit according to ~~any one of claims 1 to 5~~ claim 1,
- wherein an input terminal ~~(24a)~~ of a first cascode circuit ~~(24)~~ is coupled to said memory bit line ~~(BL)~~ and a input terminal ~~(25a)~~ of a second cascode circuit ~~(25)~~ is coupled to said reference bit line ~~(BL_R)~~.